Listing of Claims:

1. – 19. (Previously Canceled).

20. (Currently Amended) A metal-insulator-metal (MIM) capacitor structure for use in an integrated circuit, the MIM capacitor structure comprising:

(a) first and second legs extending generally parallel to one another and defining a channel therebetween, each leg including top and bottom electrodes, an insulator layer interposed between the top and bottom electrodes, and a sidewall that faces the channel; ~~and~~

(b) a first sidewall spacer extending along the channel, the first sidewall spacer including a conductive layer and a dielectric insulator layer interposed between the conductive layer and the sidewall of the first leg, wherein the conductive layer of the first sidewall spacer is physically separated from the top electrode of the first leg;

(c) a second sidewall spacer extending along the channel, the second sidewall spacer including a conductive layer and a dielectric insulator layer interposed between the conductive layer and the sidewall of the second leg, wherein the conductive layer of the second sidewall spacer is physically separated from the top electrode of the second leg; and

(d) a dielectric material disposed in the channel and interposed between the conductive layers of the first and second sidewall spacers.

21. (Original) The MIM capacitor structure of claim 20, wherein the bottom electrode for the first leg comprises titanium nitride.

22. (Original) The MIM capacitor structure of claim 21, wherein the bottom electrode for the first leg further includes an interconnect layer upon which the titanium nitride is deposited.

23. (Original) The MIM capacitor structure of claim 22, wherein the titanium nitride includes an ammonia plasma treated surface.

24. (Currently Amended) The MIM capacitor structure of claim 21, wherein the insulator layer for the first leg, and the dielectric layer in the first sidewall spacer, each comprise a high dielectric constant material.

25. (Currently Amended) The MIM capacitor structure of claim 24, wherein the high dielectric constant material in the insulator layer for the first leg and the dielectric layer in the first sidewall spacer is tantalum pentoxide.

26. (Original) The MIM capacitor structure of claim 24, wherein the top electrode for the first leg includes titanium nitride.

27. (Original) The MIM capacitor structure of claim 20, wherein the first and second legs are defined within a serpentine pattern.

28. (Original) The MIM capacitor structure of claim 20, wherein the serpentine pattern comprises at least one of a positive serpentine pattern and a negative serpentine pattern.

29. (Original) The MIM capacitor structure of claim 28, wherein the serpentine pattern comprises a positive serpentine pattern interleaved with a negative serpentine pattern.

30. – 46. (Previously Canceled).

47. (Original) A metal-insulator-metal (MIM) capacitor structure for use in an integrated circuit, the MIM capacitor structure comprising:

(a) top and bottom electrodes, wherein the bottom electrode includes an ammonia plasma treated surface; and

(b) an insulator layer interposed between the top electrode and the ammonia plasma treated surface of the bottom electrode.

48. (Original) The MIM capacitor structure of claim 47, wherein the ammonia plasma treated surface comprises titanium nitride.

49. (Original) The MIM capacitor structure of claim 48, wherein the insulator layer comprises tantalum pentoxide.

50. (Original) The MIM capacitor structure of claim 48, wherein the ammonia plasma treated surface is substantially free of titanium oxide as a result of bombardment of the ammonia plasma treated surface with nitrogen ions.

51. – 62. (Previously Canceled).

63. (New) A metal-insulator-metal (MIM) capacitor structure for use in an integrated circuit, the MIM capacitor structure comprising:

(a) a serpentine pattern including first and second legs extending generally parallel to one another and defining a channel therebetween, the serpentine pattern including a substantially co-planar top electrode, a substantially co-planar bottom electrode, and a substantially co-planar insulator layer interposed between the top and bottom electrodes, wherein the first leg includes a sidewall that faces the channel; and

(b) a sidewall spacer extending along the channel, the sidewall spacer including a conductive layer and a dielectric insulator layer interposed between the conductive layer and the sidewall of the first leg, wherein the conductive layer of the sidewall spacer is physically separated from the top electrode.

64. (New) The MIM capacitor structure of claim 63, wherein the bottom electrode comprises titanium nitride.

65. (New) The MIM capacitor structure of claim 64, wherein the bottom electrode further includes an interconnect layer upon which the titanium nitride is deposited.

66. (New) The MIM capacitor structure of claim 65, wherein the titanium nitride includes an ammonia plasma treated surface.

67. (New) The MIM capacitor structure of claim 63, wherein the insulator layer and the dielectric layer in the sidewall spacer, each comprise a high dielectric constant material.

68. (New) The MIM capacitor structure of claim 67, wherein the high dielectric constant material in the insulator layer and the dielectric layer in the sidewall spacer is tantalum pentoxide.

69. (New) The MIM capacitor structure of claim 67, wherein the top electrode includes titanium nitride.

70. (New) The MIM capacitor structure of claim 63, wherein the serpentine pattern comprises at least one of a positive serpentine pattern and a negative serpentine pattern.

71. (New) The MIM capacitor structure of claim 63, wherein the serpentine pattern comprises a positive serpentine pattern interleaved with a negative serpentine pattern.

72. (New) The MIM capacitor structure of claim 63, wherein the sidewall spacer is a first sidewall spacer, and wherein the MIM capacitor structure further comprises:

(a) a second sidewall spacer extending along the channel, the second sidewall spacer including a conductive layer and a dielectric insulator layer interposed between the conductive layer and the sidewall of the second leg, wherein the conductive layer of the second sidewall spacer is physically separated from the top electrode, and

(b) a dielectric material disposed in the channel and interposed between the conductive layers of the first and second sidewall spacers.